Remarks

Reconsideration of the rejection of claims 1-10,13-21,23, and 26-31 is requested. Claims 11,12,22,24 and 25 were allowed. Claims 32-58 stand withdrawn as directed to a non-elected invention. Claims 59-62 have been added by this amendment, and favorable consideration with respect thereto is requested.

The Specification has been amended to correct minor typographical errors. No new matter has been inserted.

Claims 14 and 15 stand rejected under 35 USC 112, second paragraph, as being indefinite for failing to particular point out and distinctly claim the invention. Examiner noted the absence of an antecedent basis for the term "barrier" in these claims.

Claims 14 and 15 have been amended to substitute the term "blocking" for "barrier" and thereby provide the proper antecedent from claim 1. The rejection has therefore been overcome.

Claims 1-3 stand rejected under 35 USC 103(a) as being unpatentable over the combination of U.S. Patent 5,258,632 issued to Sawada and U.S. Patent No. 5,788,799 issued to Steger et al. Sawada shows a velocity modulation transistor which includes "barrier" layers of AlGaAs (3,5, and 7 of Fig 2) or InAlAs (23, 25 and 27 of Fig 5). Steger et al shows an apparatus and method for cleaning surfaces of a semiconductor process chamber which utilizes multiple temperature controllable barriers.

Examiner contends that Sawada shows use of multiple dopant blocking layers, and Steger et al shows use of different temperatures for the barriers. Examiner concludes that it would have been obvious to combine the teachings of Sawada and Steger et al.

It is respectfully submitted that Examiner has not fully appreciated the distinctions of the claimed invention over the cited art.

First, it will be understood that the term "barrier layer" as generally used in the art and in the Sawada reference is not the same as a "dopant blocking layer" as used in the present claims. A "barrier layer" refers to a layer having a potential energy barrier sufficient to confine free carriers (electrons or holes) in a desired layer. In the case of Sawada's barrier layers (3,5,7 of Fig 2, and 23,25,27 of Fig 5) the layers confine electrons to their adjacent channel layers (4,6 of Fig 2, and 24,26 of Fig 5). This is shown in the energy diagram of Figs 3 and 4, and the description of the operation of the devices described, for example, at col. 4, lines 11-37, and col. 5, lines 10-25. A "dopant blocking layer" on the other hand, prevents diffusion of dopants from one layer to another. There is no teaching that Sawada's layers would be capable of blocking dopants in accordance with the claimed invention, nor would the

layers inherently have this property. The ability to block dopants would depend on several factors, including the concentration of aluminum and the temperature of formation.

Further, Steger et al's "barrier" is, in fact, a ceramic liner (102) formed over the surfaces of a deposition chamber, where the liner includes an upper and lower section (104 and 106) with separate heaters (110 and 108) so that the temperatures can be controlled independently. (See column 7, line 35 – column 8, line 15.) The different temperatures permit a different rate of removal of contaminates from the liner during cleaning. Even if Sawada could be construed as teaching the formation of blocking layers, which applicants dispute, one skilled in the art would not be guided by Steger et al to form the two layers at different temperatures. Steger et al is not concerned with forming layers over each other, nor does the existence of two temperatures have anything to do with the fabrication of an electronic device, except to clean contaminants off the apparatus walls.

Thus, the combination of Sawada and Steger et al does not teach the fabrication of a first dopant blocking layer at a first temperature and a second dopant blocking layer over the first layer at a second temperature as claimed.

Consequently, claim 1 should be allowable over the cited art.

Since claim 1 is allowable, all other claims which are dependent thereon would be allowable without the need for further discussion. Also, claim 20, which is narrower in scope, and claims 21-31 which are dependent thereon, should also be allowable.

Examiner's attention is directed to the fact that U.S. Patent No. 5,608,230 issued to Hirayama et al, U.S. Patent No. 5,753,933 issued to Morimoto, and U.S. Patent No. 6,414,340 issued to Brar, all of which were cited in the rejection of other dependent claims, are distinguishable for basically the same reasons as Sawada. That is, they describe "barrier layers" rather than "dopant blocking layers".

Examiner's attention is also directed to Morimoto at column 1, lines 48-56, wherein the prior art is described as teaching different growth temperatures for different layers. However, it is believed that this description is a recognition of the fact that a higher temperature is needed for layers including Al and therefore these temperatures would be different from InP. As far as applicants are aware, there is no teaching that InGaAlAs or InAlAs layers should be grown at different temperatures from each other. In any event, Morimoto actually teaches away from the present invention by prescribing that the layers should be grown at a constant temperature. (See column 6, lines 43-44.)

Applicants have added claims 59-62 to further distinguish over the art. Claim 59, dependent on claim 1, and claim 61, dependent on claim 20, are slightly broader than allowed claims 11,12, and 24,25 since the blocking layers are between the p-type layer and semi-insulating layers, rather than above or below those layers. This feature finds support in the Specification, for example, at page 4, lines 17-20 and in Fig 1. Claim 60, dependent upon claim 59, and claim 62, dependent upon claim 61, add the features that the p-type layer includes a Zn dopant and the semi-insulating layer includes an Fe dopant. These features find support, for example, at page 5, lines 17-23, and Figs 2 and 3. Clearly there is no teaching in the cited references that the layers are capable of blocking Zn or Fe dopants.

Passage to issue is requested.

Respectfully Submitted,

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COMPUTER RED-LINED VERSION

Amendment for Office Action dated 12/13/2002

IN THE SPECIFICATION

On page 6, lines 1-7, replace the text as follows:

--In keeping with the teaching of the above captioned parent application, a dopant barrier 112 may be used to prevent p-type dopants from diffusing out of the p-type layer 101 and into the active layer ~~104~~102. Dopant barrier 112 may be as set forth in the parent application. Alternatively, dopant barrier 112 may be aluminum spikes or aluminum containing spikes as set forth in U.S. Patent Application 09/540,474 filed March 31, 2000. This application is assigned to the assignee of the present invention, and its disclosure is specifically incorporated by reference herein.--

On page 8, lines 9-15, replace the text as follows:

--The diffusion blocking characteristics of the first dopant blocking layer 104 can be seen most readily from a review of Fig. 2. To this end, the concentration of the illustrative dopant, Zn, shown at 201, is relatively high in the layer of p-type InP (on the order of about 2 X $10^{18}/cm^3$). However, the concentration of Zn drops off significantly in the illustrative dopant blocking layer InAlAs layer 202, grown at low temperature as discussed above. The illustrative layer of InAlAs shown in Fig. ~~3~~2 is about 800Å thick, and as can be seen, the concentration of Zn drops off to minimal levels.--

IN THE CLAIMS

Please amend the claims as follows:

Claim 14 has been amended as follows:

14. (Amended) A process as recited in claim 1, wherein said first and said second dopant ~~barrier~~ blocking layers are formed by MOVPE.

Claim 15 has been amended as follows:

15. (Amended) A process as recited in claim 1, wherein said first and said second dopant ~~barrier~~ blocking layers are formed by MBE.

Add claims 59 through 62:

59. A process as recited in claim 1 wherein the first and second dopant blocking layers are disposed between a semi-insulating layer and a p-type layer.

60. A process as recited in claim 59 wherein the p-type layer includes a Zn dopant, and the semi-insulating layer includes an Fe dopant.

61. A process as recited in claim 20 wherein the first and second dopant blocking layers are disposed between a semi-insulating layer and a p-type layer.

62. A process as recited in claim 61 wherein the p-type layer includes a Zn dopant, and the semi-insulating layer includes an Fe dopant.